

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: T. HOTTA, et al  
 Serial No.: Not yet assigned  
 Filed: May 14, 2001  
 For: DATA PROCESSOR  
 Group: 2152  
 Examiner: M. Geckil



INFORMATION DISCLOSURE STATEMENT  
UNDER 37 CFR \$1.97 & 1.98

Assistant Commissioner  
 for Patents  
 Washington, D.C. 20231

May 14, 2001

Sir:

In the matter of the above-identified application, this Information Disclosure Statement is being submitted with the following citation as specified in 37 CFR \$1.97(d).

"A copy of any patent, publication or other information listed in an Information Disclosure Statement is not required to be provided if it was previously cited by or submitted to the Office in a prior application, provided that the prior application is properly identified in the statement and relied upon for an earlier filing date under 35 U.S.C. \$120."

Applicant(s) are submitting herewith a copy of Form PTO-1449 which list documents cited in parent application(s) Serial No. 07/979,772, filed November 20, 1992; which is a continuation of application Serial No. 07/433,368, filed November 8, 1989, now U.S. Patent No. 5,233,694 and related application Serial No.

07/549,916, filed July 9, 1990; Serial No. 08/149,932, filed November 10, 1993; and Serial No. 08/360,081, filed December 20, 1994.

It is respectfully requested that this information disclosure statement be considered by the Examiner.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus Deposit Account No. 01-2135 (500.28166CX2) please credit any excess fees to such deposit account.

Respectfully submitted,



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FORM PTO-1449 U.S. Department of Commerce  
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**INFORMATION DISCLOSURE  
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ATTY. DOCKET NO.

500.28166CX2

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J1011 U.S. PTO  
09/853769

05/14/01

**U.S. PATENT DOCUMENTS**

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	4 9 4 2 5 2 5	7/90	Shintani et al	395	Dig. 1	11/20/87
	5 2 8 7 4 6 5	2/94	Kurosawa et al			
	5 4 0 4 4 7 2	4/95	Kurosawa et al			
	5 5 6 1 7 7 5	10/96	Kurosawa et al			
	4 4 7 6 5 2 5	10/84	Ishii	364	Dig. 1	
	4 5 9 4 6 5 5	6/86	Hdo et al	364	DIG. 1	
	4 6 2 6 9 8 9	12/86	Rorii	395	375	
	4 6 4 4 4 6 6	2/87	Saito	395	725	
	4 7 9 4 5 1 7	12/88	Jones et al	395	725	
	4 9 1 6 6 0 6	4/90	Yamaoka et al	395	375	
	4 9 2 8 2 2 3	5/90	Dao et al	395	375	

**FOREIGN PATENT DOCUMENTS**

		DOCUMENT NUMBER							DATE	COUNTRY	CLASS	SUBCLASS	ABSTRACT	
		YES	NO											
		0	1	4	7	8	5	8	7/85	EPO				
		0	0	4	2	4	4	2	12/81	EPO				
		0	2	3	9	0	8	1	9/87	EPO				
		0	1	0	1	5	9	6	8/83	EPO				

**OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)**

J. David, "Reducing the Branch Penalty in Pipelined Processors", Computer (July 1988), pp. 47-55.
Miller et al "Floating-Duplex Decode and Execution of Instruction", IBM Technical Disclosure Bulletin, vol. 23, No. 1, June 1980, pp. 409-412.
G. Tjoden et al, "Detection and Parallel Execution of Independent Instructions", IEEE Transaction, vol. C-19, N. 10, Oct ber 1970, pp. 889-895.

EXAMINER

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	5 1 0 1 3 4 1	3/92	Circello et al	395	375	
	4 4 3 7 1 4 9	3/84	Pomerene et al			
	5 0 7 2 3 6 4	12/91	Jardine et al	395	375	5-24-89
	4 8 7 3 6 2 9	10/89	Harris et al			
	4 8 5 8 1 0 5	8/89	Kuriyama et al	395	375	3-26-87
	4 8 2 5 3 6 0	4/89	Knight, Jr.			
	4 7 8 9 9 2 5	12/88	Lahti	395	800	7-31-85
	5 0 4 3 8 6 8	8/91	Kitamura et al	395	775	12-24-87

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DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	ABSTRACT
					YES NO
4 5 9 2 3 2	12/91	EPO			
3 2 8 8 2 4 6	12/91	Japan			XX
4 5 5 9 6 6	11/91	EPO			
6 3 1 3 1 2 3 0	6/88	Japan			

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	D. Ditzel, et al "The Hardware Architecture of the Crisp Microprocessor" ACM, 0084-7495, pp. 309-319.
	Capozzi et al, "Non-sequential High-performance Processing", IBM Technical Disclosure Bulletin, vol. 27, No. 5, 10/84, pp. 2842-2844.

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	4 6 2 0 2 7 5	10/86	Wallach et al	395	800	
	3 6 1 4 7 4 5	10/71	Podia et al	395	650	
	4 9 2 8 2 2 6	5/90	Kamada et al	364	200	
	3 7 7 1 1 3 8	11/73	Celtruda et al			
	4 6 7 7 5 4 5	6/87	Blahut			

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8 8 0 9 0 3 5	11/88	WIPO			
0 0 8 2 9 0 3	7/83	EPO			
6 3 7 3 3 3 2	2/88	Japan			XX

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	O. Serlin, "The Serlin Report on Parallel Processing", ITOM International Co., Issue No. 7, 12/87, pp. 10-18.
	IEEE Journal of Solid-State Circuits, "MIPS-X: A 20-MIPS Peak 32-Bit Microprocessor with on-chip Cache", Horowitz, et al, vol. sc-22, No. 5, October 1987, New York.
	J. Bond, "Parallel Processing Concepts Finally come together in Real Systems", Computer Design, June 1, 1987, pp. 51-74.

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